REMARKS

This application has been carefully reviewed in light of the Official Action dated August 11, 2004 that the Examiner indicated to be a FINAL Official Action, and also in light of the Advisory Action dated January 26, 2005, wherein the Examiner refused to enter Applicant's Amendment After Final Rejection Under 37 CFR 1.116. It is respectfully requested that the foregoing Amendment Accompanying Request For Continued Examination be entered and considered by the Examiner prior to the issuance of a further Official Action in this case.

Claims 1-24 were pending in this application at the time of the issuance of the currently outstanding Official Action. By the foregoing Amendment, Claims 1, 2, 3, 5, 7, 9, 11,13, 15, 17 and 19 have been amended. Claim 8 has been cancelled, without prejudice. No claims have been added. Accordingly, upon the entry to the foregoing Amendment, Claims 1-7 and 9-24 as hereinabove amended will constitute the claims pending in this application.

In the currently outstanding Official Action, the Examiner has:

1. Acknowledged Applicants claim for foreign priority under 35 USC 119(a)-(d) or (f), and confirmed the receipt of the required copies of the priority documents for this application by the United States Patent and Trademark Office;

2. Provided Applicants with a copy of the Form PTO-1449 that accompanied their Information Disclosure Statement of 30 April 2004 duly signed, dated and initialed by the Examiner in confirmation of his consideration of the art listed therein, and with the Advisory Action of 26 January 2005 provided Applicants with copies of the Form PTO-1449 that accompanied their Information Disclosure Statement of 25 September 2003 and the Form PTO/SB/08a/b that accompanied their Information Disclosure Statement of 25 August 2004 both duly signed, dated and initialed by the Examiner in confirmation of his consideration of the art listed therein; **but failed to provide Applicants with a copy of the Form PTO/SB/08a/b that accompanied their Information Disclosure Statement of January 29, 2005 duly signed, dated and initialed by the Examiner to confirm his consideration of the art listed therein – appropriate confirmation of the receipt and consideration of Applicants' Information Disclosure Statement of January 28, 2005 in response to this communication is respectfully requested**;

3. Indicated that the drawings filed as on 20 May 2004 are accepted;

4. Provided Applicants with a Notice of References Cited (Form PTO-892) and a copy of the reference cited therein;

5. Rejected Claims 1 and 2 under 35 USC 102(e) as being unpatentable over US Patent 6,426,670 to Tanaka;

6. Rejected Claim 5 and 6 under 35 USC 102(e) as being unpatentable over US Patent 6,549,196 to Taguchi, et al;

7. Rejected Claim 3 under 35 USC 103(a) as being unpatentable over the combination of the Tanaka reference and US Patent 6,580,359 to Tam;

8. Rejected Claims 7 and 8 under 35 USC 103(a) as being unpatentable over the Taguchi, et al reference;

9. Rejected Claim 4 under 35 USC 103(a) as being unpatentable over the Tanaka reference in view of the Tam reference further in view of the Taguchi, et al reference;

10. Rejected Claim 9 on the same grounds as the rejection of Claims 2-8;

11. Rejected Claims 11 and 13 on the same grounds as the rejection of Claims 1-4;

12. Rejected Claims 12, 14, 16, 18 and 21 apparently under 35 USC 103(a) based upon his previous rejections and an assertion that power savings advantages would have made it obvious to one skilled in the art to include the claimed display circuit in a portable device of the type known in the art;

13. Rejected Claim 15 on the same grounds as stated with respect to Claims 5 and 6 in view of the disclosure in Taguchi et al of how to incorporate the signal circuit into the matrix display;

14. Rejected Claim 17 on the same grounds as stated with respect to Claims 7 and 8;

15. Rejected Claim 19 on the same grounds as stated with respect to Claim 9 in view of the disclosure in Taguchi et al of how to incorporate the signal circuit into the matrix display;

16. Indicated that Claims 10 and 22-24 are allowed;

17. Indicated that Claim 20 would be allowable if rewritten in independent form including all of the limitations of its base claim and any intervening claims; and,

18. Cited, but failed to apply against any of the pending claims of this application an additional references that is deemed to be pertinent to Applicants' disclosure.

With respect to items 1-4, 16, 17 and 18, Applicants respectfully submit that no further comment in these Remarks is required.

In general, Applicants' response to the currently outstanding substantive rejections of the claims of the above-identified application is that (i) the references when fully considered and understood do not support the Examiner's characterizations of them, and/or (ii) the references are insufficient to establish the *prima facie* case of unpatentability that the Examiner is required to supply in support of his rejections.

In this regard, Applicants have previously pointed out that the present invention has the objectives of reducing power consumption in a signal line drive circuit without adverse impact upon the operating characteristics thereof; providing an image display device that utilizes that signal line drive circuit; and providing portable apparatus utilizing that signal line drive circuit.

Further, Applicants have noted that to accomplish these objectives the present invention (i) eliminates an unnecessary circuit from prior art configurations, (ii) eliminates the current that would otherwise be used in the eliminated circuit, and (iii) avoids the occurrence of charging/discharging stray capacitance between bus lines when the image signal represents a small number of tones.

Applicants again respectfully submit that the cited references are taken from totally different technical fields relative to the technical field of the present invention and/or do not either alone or in combination with one another teach, disclose or suggest the present invention as a means of accomplishing the above-stated objectives. In other words, Applicant respectfully submits that the Examiner has not fully considered ***all*** of the limitations of each of the present claims and also has not considered the ***contexts*** in which the various elements of those claims alleged to be disclosed in the prior art are, in fact, disclosed therein during the course of making his rejections. Thus, for example, it is Applicants' position that the presence of a switch associated with a buffer located between a voltage division circuit and a chooser circuit in the prior art relied upon would only be relevant to the present invention to the extent that that switch performs the same function in the reference circuit as it does in the present invention. Otherwise, such a rejection can only be characterized as improper hindsight based upon the Applicants' disclosure.

Accordingly, as will appear more fully below, Applicants respectfully submit that in light of the foregoing amendment, the currently outstanding rejections of the claims of this application should be reconsidered and withdrawn, and that Claims 1-7 and 9-24 as hereinabove amended should be allowed.

The Examiner indicates in the currently outstanding Official Action, however, that Applicants' have heretofore relied upon means-plus-function arguments in the support of the patentability of the claims of this application, and also that such a means –plus-function argument is insufficient to overcome the Examiner's rejections. Specifically, the Examiner indicates that where the function argued is not specifically stated in the claims and the art shows the structure claimed ***regardless of the function of the structure in the device taught by the prior art in which it appears*** the claim at issue is not patentable over that art. Applicants do not agree and respectfully request reconsideration in view of the foregoing Amendment and the following comments.

With reference to item 5 above, the Examiner has rejected Claims 1 and 2 under 35 USC 102(e) as being anticipated by the Tanaka reference. In this regard, Applicants note that the Examiner now has clarified the fact that he is relying upon Figure 1 of the Tanaka reference as the basis for his rejection of Claim 1. Specifically, the Examiner now indicates he believes that Figure 1 of the Tanaka reference shows a reference voltage chooser (item 13) where the first reference voltage is directly (v1 and v5) submitted to the selecting circuit. Further, the Examiner indicates that Tanaka also shows a second reference voltage produced through a voltage divider and then buffered to the selection circuit.

As hereinabove amended, a main feature of the invention according to Claim 1 is that the claimed structure includes a reference voltage line directly inputting (directly transmitting) ***multiple*** first reference voltages supplied by external reference voltage supply means to a reference voltage chooser circuit. With that arrangement, no buffer circuit is required for the reference voltage line directly transmitting the first reference voltages. Therefore, the signal line drive circuit takes up a smaller area and eliminates the amount of current that would otherwise be utilized by a buffer circuit. This results in power savings by the claimed signal line drive circuit in comparison to the prior art.

Similarly, as above amended, a main feature of the present invention according to Claim 2 is that a second reference voltage produced by voltage division from at least two of ***multiple*** first reference voltages is supplied to the reference voltage chooser circuit via a buffer circuit having a high input impedance and a low output impedance, the ***multiple*** first reference voltages are directly inputted (directly transmitted) to the reference voltage chooser circuit, and the reference voltage chooser circuit chooses input voltages in accordance with the tones represented by the image signal and thereafter outputs the chosen voltages as a signal line drive signals. Hence, it will be understood that a main feature of claim 11 (see item 11 above) is to include the foregoing features of Claim 2 in a display device.

In this case as well, no buffer circuits are required for the reference voltage lines directly transmitting the multiple first reference voltages to the reference voltage chooser circuit. Thus, the signal line drive circuit occupies a smaller area and eliminates the amount of current that otherwise would be expended in a buffer circuit. A power saving in the signal line drive circuit is the result.

More particularly, Figure 1 of the Tanaka reference shows a reference voltage line directly transmitting a first reference voltage Vdd to the reference chooser circuit 13 as required by Claim 1 of this application. However, unless ground can be taken as a first reference voltage ***from external voltage supply means*** (as necessarily must follow from the Examiner's argument, see Tanaka, Fig. 1 at V5), the Tanaka reference does not disclose that more than one (i.e., ***multiple*** "first reference voltages" ***from external voltage supply means***) are supplied directly to the signal line drive circuit from which a resistance type voltage divider circuit creates the "second reference voltages" as is hereinabove specifically claimed as an explicit statement of a heretofore inherent limitation of the claim.

Similarly, amended Claim 2 requires a "second reference voltage produced by voltage division ***from at least two*** of the ***multiple*** first reference voltages" and that "***multiple*** first reference voltages ***from external voltage supply means*** are directly supplied to the reference voltage chooser circuit". The foregoing amendment, therefore, also clarifies the heretofore inherent fact that Claims 1 and 2 contemplate (and have throughout this prosecution contemplated) that in the present invention ***multiple*** first reference voltages are to be input from external voltage source means, **not ground**.

Consequently, it will be understood that the present invention differs from the Tanaka reference in that the multiple (i.e., all) of the first reference voltages are directly supplied to the reference voltage chooser circuit from external voltage supply means, whereas in the Tanaka reference one of the comparable reference voltages is fixed at ground. Applicants respectfully submit that the specification of an external voltage supply means as the source of all of the input first reference voltages is inconsistent with the supply of ground potential in the context of this application. Indeed, the fixing of one of the reference voltages at ground potential as in Tanaka limits the settings of the applied voltages to the liquid crystal thereby making it impossible to apply the suitable (desired) voltages contemplated by the present invention to the liquid crystal.

Hence, Applicants respectfully submit that since the Tanaka reference in its Fig. 1 and the related description discloses the application of only a single first reference voltage ***from an external reference voltage source***, the Tanaka reference cannot anticipate either Claim 1 or Claim 2 as hereinabove amended under 35 USC 102 either from a structural point of view or from the functional/contextual considerations argued previously and mentioned above.

With respect to item 6 above, the Examiner has Rejected Claim 5 and 6 under 35 USC 102(e) as being unpatentable over US Patent 6,549,196 to Taguchi, et al. A main feature of claim 5 is that ***a second switch controlled by a second control signal is provided between a reference voltage line(s) supplying the first reference voltages from external voltage supply means and the voltage divider circuit that produces a second reference voltage*** by voltage division from at least two of the first reference voltages. Item 13 above deals with the fact that Claim 15 embodies these features in a display device. Here again it is possible to eliminate an amount of current that would otherwise occur in the portion of a prior art voltage divider circuit that is not being used in the present invention thereby realizing a power savings in the signal line drive circuit.

In particular, with respect to Claim 5, the Examiner relies upon Fig. 11 of the Taguchi reference as disclosing the presently claimed structure. Applicants respectfully note, however, that Claim 5 calls for "***a*** voltage divider circuit for producing a second reference voltage by voltage division from ***at least two*** first reference voltages from external voltage supply means" and "a second switch ... interposed between the first reference voltages and the voltage divider circuit". In Taguchi's Fig. 11, however, there are ***two*** voltage division circuits, one providing voltage division between input voltage VDD1 and ground, and the other providing voltage division between input voltage VDD2 and ground. Further, contrary to the claims of this application, only the second of the Taguchi voltage divider circuits has a switch located between the input voltage VDD2 and the remainder of the circuit (i.e., all of the first reference voltages are not separated from a single voltage divider by switches).

The various other switches disclosed in Taguchi's Fig. 11 control whether a second reference from the VDD1 circuit, a second reference voltage from the VDD2 circuit, or neither of them is provided to the chooser circuit 3. Thus, Taguchi does not disclose a voltage divider circuit for producing a second reference voltage from at least two reference voltages separated therefrom by switches. Instead, in Taguchi, the various second reference voltages are separately produced from each of two distinct voltage division circuits according to the dictates of the remainder of the circuit.

Still further, as argued in the previous amendment in this application, the Taguchi et al reference discloses a D/A conversion circuit that is provided with switches SW11 through SW18, and three types of current changeover switches SW1 through SW3. The switches SW11 through SW18 are for dividing the output of the reference power supply so as to select the voltages to be supplied to the output buffer. In addition, the current changeover switches SW1 through SW3 are provided for selecting one of the voltages divided from the output voltage and a voltage from the pre-buffer as a voltage to be supplied to the output buffer. In other words, the switches provided in the D/A conversion circuit of the Taguchi et al reference are not provided for eliminating an amount of current that would otherwise occur in a circuit that is not being used in their arrangement (i.e., for cutting the power input to the buffers as presently claimed). Rather, those switches are provided for selecting (switching) the voltage to be supplied to the output buffer according to the contextual demands of the remainder of the Taguchi circuit and therefore are not comparable to the switches of the presently claimed invention.

Accordingly, Applicants again respectfully submit that the Examiner's argument in support of his outstanding rejection of Claims 5, 6 and 15 fails both from a structural point of view and from a functional point of view. Reconsideration and allowance of these previously considered issues in view of the foregoing amended claim language is respectfully requested.

With respect to item 7 above, Claim 3 is rejected under 35 USC 103(a) as being unpatentable over the combination of the Tanaka reference and US Patent 6,580,359 to Tam. A main feature of the invention according to Claim 3 is that a second reference voltage produced by voltage division from at least two of the first reference voltages from external voltage supply means is supplied to the reference voltage chooser circuit via a buffer circuit having a high input impedance and a low output impedance, ***a power supply voltage is supplied to the buffer circuit via a first switch controlled by a first control signal***, and the reference voltage chooser circuit chooses input voltages in accordance with the tones represented by the image signal and thereafter outputs the chosen voltages as the signal line drive signals. A main feature of claim 13 is to include the foregoing features of Claim 3 in a display device. Again, in either of these cases, it is possible to eliminate the amount of current that would otherwise occur in the buffer circuit not being used and thereby to realize power savings in the signal line drive circuit.

The Taguchi reference has been discussed above. Despite this discussion, however, the Examiner asserts that the only part of Claim 3 missing from Taguchi is the concept of energy conservation for inactive buffers. According to the Examiner, the Tam reference (U.S. Patent No. 6,580,351) recognizes that buffers consume power and that buffer selection control can save power. ***As abstract propositions***, these statements by the Examiner may be true. Nevertheless, Applicants respectfully submit that the Examiner's implied assertion that one skilled in the art could (and/or would) simply add the Tam selective buffer control system to the Taguchi reference so as to arrive at the present invention takes the point too far.

The Tam reference relates to a selectable input buffer control system, not a signal line drive circuit as herein claimed. In particular, Tam discloses a crosspoint switch 10 in which a plurality of input cells 22 are arranged in a matrix manner such that each cell provides an output only when it receives an input via its associated input bus ***and*** is appropriately addressed by its associated address bus. This is to be distinguished from the present invention wherein input power is provided only from an associated power supply.

Accordingly, it will be understood that the crosspoint switch 10 is for selecting signals received from the selectable input buffer control system 12 in accordance with two different inputs supplied thereto so as to output the signals so selected to output buffers 82, 84, 86 and 88 (see, column 4, lines 18-25). In other words, ***the crosspoint switch 10 in the Tam reference is not provided for eliminating the amount of current that would occur in a circuit not being used in the arrangement disclosed, but rather is merely for selecting (switching) signals to be outputted to the output buffers 82, 84, 86 and 88.*** Applicants have found no disclosure in the Tam reference to the effect that ***power supply input*** to the output buffers is supplied via a first switch controlled by a first control signal as herein claimed. Instead, as far as Applicants can tell from the Tam disclosure, the output signals that are supplied to the output buffers are selected in the input buffer control system 12 as discussed above, and thereafter fed to the various output buffers via the crosspoint switch 10 without the intervention of a power supply switch controlled by a first control signal as herein claimed.

In other words, Applicants have found nothing specifically disclosed in the Tam reference that controls any other power input to the output buffers than the crosspoint switch 10. ***Accordingly, Applicants respectfully submit that contrary to the Examiner's assertion in the currently outstanding Official Action, a simple insertion of the Tam device into the Taguchi device would not result in the present invention as presently claimed in Claim 3 even in the event that the distinctions between the present invention and Taguchi discussed hereinabove were not present.***

Accordingly, the selectable input buffer control system of the Tam reference has an arrangement that is totally different from that of the signal drive circuit and other circuits of the present invention. Further, the Examiner's attempt to combine the Tam and Taguchi references so as to render the presently claimed invention obvious clearly fails because all of the elements of the present invention co-operating with one another in the manner of the present invention are not disclosed by the cited combination of references (i.e., neither the structure, nor the function of the structure, of the present invention is disclosed, taught or suggested by the combination of references relied upon by the Examiner). In this regard, reference to the foregoing discussion of the differences in structure between the Taguchi reference and the invention as claimed hereinabove is again significant.

Still further, the generalized nature of the Examiner's use of the Tam reference as supplying claimed elements missing from the Taguchi reference is such as to leave the Applicants to guess concerning the particulars of how the Examiner intends to apply the general concepts of the Tam reference to, or combine (or incorporate them in) the other references. Consequently, Applicants respectfully submit that absent some further detailed notice concerning the nature of the combination of the Taguchi and Tam references that is envisioned by the Examiner, the present rejection of Claim 3 also must fail because it is so nonspecific that Applicants cannot effectively respond. Applicants cannot be forced to "guess" as to the meaning of the rejection.

With regard to item 9 above, Claim 4 is dependent upon Claims 3. Accordingly, to the extent that Claim 3 is patentable, Claim 4 is patentable as well.

With respect to item 8 above, the Examiner has rejected Claims 7 and 8 under 35 USC 103(a) as being unpatentable over the Taguchi, et al reference. By the foregoing Amendment, Applicants Have amended Claim 7 so as to include the features that a sampling signal is generated that is indicative of the tones in the image signal, and "the decoder circuit is controlled through a third control signal according to a decoder table determined by the number of tones represented by the sampling signal". Further, Applicants have cancelled Claim 8, without prejudice, as being largely redundant in view of amended Claim 7.

It will be seen that upon the entry of the foregoing amendment, a main feature of claim 7 will be that ***a decoder circuit*** controlling the reference voltage chooser circuit ***is controlled through a third control signal to change a decoder table determined by the number of tones represented by a sampling signal generated by a sampling of the image signal***, whereby the reference voltage chooser circuit changes a reference voltage choosing pattern of the signal line driving circuit. Claim 17 is amended so as to incorporate these features into the display device therein claimed. In either case, however, it will be understood that the decoder table can be changed in accordance with the number of tones represented by the image signal. Consequently, the signals transmitted by the bus lines are fixed when the image signal represents a small number of tones. This fixation prevents the occurrence of the charging/discharging of stray capacitances between the bus lines thereby also reducing the power consumption of the signal line driving circuit.

Applicants respectfully submit that the Taguchi et al reference fails to disclose, teach or suggest the present invention as set forth in amended Claim 7 (or 17) above. Further, Applicants respectfully note that the Examiner appears to agree with this conclusion in that he expressly admits that the Taguchi reference fails to teach a decoder wherein the decoder table can be modified. It is true that the Examiner suggests that (i) the idea of having a decoder with a plurality of decoder tables is "extremely conventional" in the art, (ii) that that concept therefore cannot be considered as being novel, and (iii) that one of ordinary skill in the art would have been motivated to utilize that concept in the present invention in order to better accommodate increased versatility in interpreting and displaying image signals. As will appear more fully below, however, Applicants respectfully submit that the Examiner's logic, while seemingly appealing in the abstract, nevertheless fails to establish a *prima facie* case in support of the Examiner's position based upon teachings found within the "four corners" of the cited prior art to which Applicants can effectively reply.

The decoders in the Taguchi reference are operated in accordance with an arbitrary digital sequence established for the pixels of the display, not in accordance in accordance with a signal representative of the tones of a sampled image. This is because Taguchi et al is concerned with digital/analog transformation of input signals in accord with a pre-established digital pattern of a pixel/display. The present invention is not doing the same thing to accomplish the same objective as the Taguchi et al reference. Consequently, Applicants respectfully submit that the intuitive conclusion that the Examiner has set forth in the currently outstanding Official Action is not shown, taught or suggested by the cited references, but rather is an exercise of improper "hindsight" analysis based upon Applicants' specification. Applicants respectfully submit that such a basis for rejection should not be allowed to stand.

With respect to the other specifically enumerated items above, Applicants respectfully note that Claims 9 and 10 represent combinations of the invention according to claims 3, 5 and 7. Similarly, Claim 19 represents a combination of the inventions according to Claims 13, 15 and 17. Therefore, it will be readily recognized that the inventions according to claims 9 and 19 also produce the effects just discussed according to the particular combinations of features embodied thereby.

In summary, therefore, Applicant respectfully notes that the Examiner has taken the position that since the functional benefits associated with the present invention are not stated in the claims (***even though the functions of the various element are stated specifically***) and the cited art shows generally similar structures to the structure herein claimed, Applicants have failed to overcome his stated grounds of rejection. However, Applicants respectfully submit that the Examiner has stretched the logic supporting his outstanding rejections too far.

In particular, the Examiner has disregarded specific claim limitations (that by definition must be deemed to be material) in applying (i) elements disclosed in quite distinct contexts from the present invention, and (ii) broad and unspecific constructions of the cited art against the present claims.

Accordingly, as will be clear from the following discussion of the relevant law, Applicants respectfully submit that while the Examiner perhaps is correct in his suggestion that the structures disclosed in the cited art are at least arguably relevant to the field of the present invention, the Examiner nevertheless oversteps the proper bounds of rejection in his attempt to equate particular elements of the cited art to particular elements of the present claims. This is particularly true in those cases in which the specifically defined functional usage of the reference structure relied upon does not conform to the explicit function of the part of the claim that the Examiner alleges that it anticipates or renders obvious.

Hence, Applicants respectfully submit that the Examiner exceeds the proper scope of analysis at the points of his rejections at which he disregards the specific and material limitations of the present claims not found in (or suggested by) the cited art (i.e., what the elements of the claims are "for"). This, in addition to the nonspecific and generalized application of alleged teachings of the prior art and so-called "well know" concepts to those of ordinary skill in the art without any reference to tangible support for the positions being taken to which Applicants could effectively respond are respectfully submitted to be insufficient to support the Examiner's outstanding claim rejections.

The legal standards to be applied in this situation are clear. Further, it is noted that the Examiner has not challenged Applicants' previous statement thereof. These standards are repeated below.

With respect to anticipation, the law is clear that "a claim is anticipated only if each and every element ***as set forth in the claim*** is found either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Company of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) The ***identical invention*** must be shown in as complete detail as contained in the...claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) The elements must be arranged as required by the claim... *In re Bond,* 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990) *Emphasis added.*

As discussed in detail above, the cited references do not satisfy these standards because none of those references disclose all of the components (claimed features/limitations) of the present invention functioning in the same way relative to one another as herein claimed.

With respect to the Examiner's rejections under Section 103 of Title 35 United States Code, it is settled that:

> To establish a *prima facie* case of obviousness under Section 103, Title 35 United States Code (35 US §103), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2D 1438 (Fed. Cir. 1991).

Hence, the test under 35 USC 103 is not "obvious to try", nor is it whether or not the claimed invention could be assembled utilizing various components derived from divergent pieces of prior art (i.e., utilizing the claim as a framework for the assembly of a mosaic into which various divergent elements of the prior art are fit without any suggestion in the prior art itself rather than the Applicant's disclosures to do so).

In view of the above discussion, therefore, Applicants respectfully submit that the currently outstanding rejections are insufficient to preclude the patentability of the claims of this application as hereinabove amended. Specifically, the claims are not anticipated because all of their elements co-operating with one another in the manner claimed are to be found in the cited art.

Furthermore, the claims are not obvious in view of the cited art because the cited art (i) fails to provide any suggestion or motivation for its combination in the manner herein claimed, (ii) fails to carry any reasonable indication of the success of the claimed combination because it deals with totally different problems in different contexts that that of the present invention, and (iii) it does not (absent reference to Applicants' specification) teach or suggest all of the limitations of the present claims as has been demonstrated in detail by the foregoing discussion.

For each and all of the foregoing reasons, Applicants respectfully submit that that the references relied upon by the Examiner when fully considered as to their true content do not support the Examiner's characterizations of them. In addition, Applicants respectfully submit that the references relied upon by the Examiner are insufficient, whether taken alone or in combination with one another, to establish a *prima facie* case supporting the Examiner's assertion that the claims of this application as hereinabove amended are not patentable.

Consequently, in view of the foregoing Amendment and Remarks, Applicants respectfully submit that the claims of this application as hereinabove amended are in condition for allowance. Therefore, entry of the foregoing Amendment, reconsideration and allowance of the claims of this application as set forth hereinabove in response to this communication is respectfully requested.

Finally, Applicants believe that additional fees are not required for consideration of the foregoing Amendment After Final Rejection Under 37 CFR 1.116. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105** therefor.

Respectfully submitted,

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